## AMENDMENTS TO THE CLAIMS

1    1.    (Currently Amended) A method for verifying scan chain equivalency
2    between two representations of a circuit design having at least one scannable state
3    element, at least one scan-out pin and at least one output pin, comprising:
4        for each representation of the circuit design, loading each scannable state element
5            with a symbolic expression that characterizes a logical location of said
6            scannable element in the circuit design; and
7        for each representation of the circuit design, performing a scan shift operation to
8            verify a content value for each [the] scannable state_ [-]element [contents]
9            at said scan-out pin and said output pin of the design.

1    2.    (Original)    The method of claim 1, wherein the two representations of
2    a circuit design comprise a switch-level netlist and an RTL netlist.

1    3.    (Original)    The method of claim 1, wherein the two representations of
2    a circuit design comprise a transistor level implementation and a behavioral level
3    description.

1    4.    (Original)    The method of claim 1, wherein the two representations of
2    a circuit design comprise RTL and schematic models of a memory circuit.

1    5.    (Original)    The method of claim 1, wherein the two representations of
2    a circuit design comprise a first RTL model of a storage circuit and a second RTL model
3    of a storage circuit.

1    6.    (Original)    The method of claim 1, wherein the two representations of
2    a circuit design comprise a SPICE-level netlist and a gate level description.

1    7.    (Original)    The method of claim 1, wherein said loading of each
2    scannable state element with a symbolic expression comprises simulating said circuit
3    design in a functional mode for a first minimum threshold number of cycles by applying
4    symbolic expressions to at least a first input for said circuit design.

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1      8.    (Previously Presented)    The method of claim 7, wherein said first
2 minimum threshold number comprises a maximum sequential depth of all scannable
3 state-elements on all paths from all primary inputs in said circuit design.

1      9.    (Original)    The method of claim 1, wherein said loading and
2 performing steps are implemented with a symbolic simulator to check scan chain
3 equivalency with respect to complete scan chain connectivity from primary input to
4 primary output, logical location of all scannable state elements, scan chain length and
5 scan chain order.

1      10.    (Original)    The method of claim 1, wherein said loading and
2 performing steps are implemented with a symbolic simulator to obtain complete
3 coverage.

1      11.    (Original)    The method of claim 1, wherein said scan shift operation
2 comprises simulating a sequence of scan clocks equal to a multiple of the number of
3 scannable state-elements in the circuit design.

1      12-20. (Cancelled)

1      21.    (Previously Presented)    A method for verifying scan chain
2 equivalency between two representations of a circuit design having at least one scannable
3 state element, at least one scan-out pin and at least one output pin, comprising:
4    for each representation of the circuit design, loading each scannable state element
5      with a symbolic expression that characterizes a logical location of said
6      scannable element in the circuit design;
7    for each representation of the circuit design, performing a scan shift operation to
8      generate scan-out pin values at said scan-out pin; and
9    comparing scan-out pin values from each representation of the circuit design to
10      verify scan chain equivalency between the two representations of the
11      circuit design.

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